With respect to paragraph 1 of the Office Action, corrected formal drawings have been filed herewith.

Claims 1, 5, 7, 8, 9, 11 and 24 stand objected to for non-substantive formality reasons in paragraph 2 of the Office Action. It is respectfully submitted that claim changes herein address and overcome any potential issue in this respect.

Section 112 Rejection of Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 112, first paragraph (see paragraph 3 of the Office Action). In particular, the Office Action contends that the specification as filed does not support the "fully depleted" aspect of claim 1. This Section 112, first paragraph, rejection is clearly incorrect and is respectfully traversed for at least the following reasons.

The instant specification as filed clearly describes depletion between a channel in each MOS transistor and a part underlying the channel (e.g., pg. 24, lines 2-4). Moreover, the instant specification as filed explains that the depletion of the instant invention is "*complete depletion*" (e.g., pg. 11, lines 3-4). Since "complete depletion" is clearly described in the application as filed, the claim is supported and the Section 112 rejection should be withdrawn.

Art Rejection of Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Mitani (newly cited WO99/27585 – see also apparent US counterpart 6,392,277) in view of KR '470 (KR 96-12470). Since the US counterpart (Mitani '277) is in English, it is referred to herein for purposes of simplicity and understanding. This

Section 103(a) rejection of claim 1 is respectfully traversed for at least the following reasons.

Claim 1 requires that "the contact portion for applying the different bias voltages is formed in a device isolation region and comprises a contact hole in the semiconductor layer and the buried insulating film, said contact hole reaching the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer, and wherein a conductor of the contact portion in the contact hole is electrically insulated from the semiconductor layer by at least said device isolation region which includes at least one insulator; and . . . . bias voltages applied via separate of said contact portions for both of the first and second transistors are changed between the active and standby states so that active regions of the first and second transistors are completely depleted simultaneously in the standby state." For example, Fig. 3 of the instant application illustrates that conductor 37b of the contact portion in the contact hole is electrically isolated from semiconductor layer 33 by at least the device isolation region 37a and/or the like. Moreover, claim 1 also requires, for example, controlling the bias voltage for PMOS and NMOS transistors on the same substrate between the active and standby state(s) so that active regions of the transistors are *fully depleted simultaneously in the standby state*. The cited art fails to disclose or suggest each of the aforesaid underlined aspects of claim 1.

Mitani '277 (the US counterpart is referred to herein since it is in English) in Fig. 8 discloses an n-conduction type transistor Qn formed on semiconductor substrate 20A. The n-conduction type transistor Qn includes n-type source/drain regions 28 defined in

the semiconductor layer, a p-type channel, gate insulator 22 and gate electrode 27 (e.g., see from col. 9, line 65 to col. 10, line 11). A p-type region 24A is provided as a back gate. An *interconnect 33D provides interconnection between and supplies the same potential to both the semiconductor layer (region 31) and back gate 24A*. It can be seen that Mitani significantly differs from the invention of claim 1 in at least the following two respects.

First, as explained above, interconnect 33D in Fig. 8 of Mitani provides interconnection between and supplies the same potential to both the semiconductor layer (region 31) and back gate 24A. In other words, interconnect 33D is in electrical communication with both back gate 24A and the semiconductor layer of the SOI substrate, and is provided in order to supply the same electric potential to both. In direct contrast with Mitani, the invention of claim 1 intentionally isolates the contact for high concentration impurity diffusion layer 31a (an alleged back gate) from the semiconductor layer of the SOI substrate via isolation region 37a. In this respect, claim 1 expressly states that "a conductor of the contact portion in the contact hole is electrically insulated from the semiconductor layer by at least said device isolation region which includes at least one insulator." Mitani fails to disclose or suggest this aspect of claim 1.

Moreover, the recitation of the aforesaid "insulated" structure of claim 1 may provide for significant technical advantages over the undesirable structure of Mitani in this respect. Because the contact portion and the semiconductor layer are electrically insulated as recited in claim 1, the magnitude of the bias voltage may be controlled for each well when a number of wells are formed in the semiconductor layer 31. Moreover,

this "insulated" aspect of claim 1 also allows for the threshold value to be easily controlled by applying the voltage only from the well side. In contrast, Mitani has very poor control over the threshold value since the same voltage is applied from both the back gate and the semiconductor layer. Mitani is highly undesirable in this respect. Still further, when the contact portion is not insulated from the semiconductor layer (as in Mitani), the charge in the S/D region tends to form a leak path from the well to the substrate via the contact thereby rendering a well bias to be controlled depending upon an ON/OFF state of the transistor. In contrast, the invention of claim 1 which electrically insulates the conductor of the contact portion from the semiconductor layer allows for control of the threshold voltage of the transistor by applying different bias voltages depending upon an ON/OFF state thus making it possible to realize a transistor having reduced leak path(s), less power consumption and/or higher controllability. Yet another advantage of electrically insulating the conductor of the contact portion from the semiconductor layer is that instability of current on switching the transistor can be reduced since the well bias may be controlled independent of the source/drain region. Thus, not only does Mitani fail to disclose or suggest electrically insulating the conductor of the contact portion from the semiconductor layer as required by claim 1, but Mitani is technically disadvantageous in this respect for the aforesaid reasons.

Second, Mitani fails to disclose or suggest that bias voltages are applied to first and second transistors Qn and Qp and are changed between the active and standby states so that active regions of both transistors are *completely depleted simultaneously in the*

standby state as called for in claim 1. The Office Action's contention that this is inherent is unsupported and lacks merit.

For each of the aforesaid reasons, it can be seen that Mitani is entirely unrelated to the invention of claim 1. Moreover, citation to KR '470 cannot overcome the aforesaid fundamental flaws of Mitani. *One of ordinary skill in the art would never have used the contact isolation region of KR '470 in Mitani because it would insulate the back gate contact from the semiconductor layer which would in turn destroy the functionality and purpose of Mitani.* Such a combination would clearly be improper under Section 103(a) as a matter of law. Moreover, even if such a combination were made (which applicant believes would be clearly incorrect), the invention of claim 1 still would not be met for the second reason discussed above.

Art Rejection of Claim 7

Claim 7 requires that "a conductor of the contact portion in the contact region is electrically insulated from said semiconductor layer; and a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltages applied via separate contact regions for both of the first and second transistors are changed between the active and standby states so that active regions of the first and second transistors are completely depleted simultaneously in the standby state." Again, the cited art fails to disclose or suggest these aspects of claim 7.

Art Rejection of Claim 24

Claim 24 requires "respective contact portions for applying to the semiconductor substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are completely depleted simultaneously in the standby state, wherein said contact portions are electrically insulated from said semiconductor layer." Again, the cited art fails to disclose or suggest the aforesaid aspects of claim 24.

Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are allowable. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (*Amended*) A semiconductor device comprising:

a first MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,

a contact portion for applying to the semiconductor substrate different bias voltages in an operating state and a standby state of a semiconductor circuit including the first MOS transistor,

the first MOS transistor including source and drain regions of a second conductivity type, a channel of the first conductivity type, and wherein an impurity diffusion layer of the first conductivity type is formed in the semiconductor substrate under at least the entire source, drain and channel regions, so that the impurity diffusion layer is of the same conductivity type as the semiconductor substrate, wherein said source and drain regions as well as said channel are all formed in the semiconductor layer,

wherein the contact portion for applying the different bias voltages is formed in a device isolation region and comprises a contact hole in the semiconductor layer and the buried insulating film, said contact hole reaching the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer, and wherein a conductor of the contact portion in the contact hole is electrically insulated

from the semiconductor layer by at least said device isolation region which includes at least one insulator; and

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltages applied via separate of said contact portions for both of the first and second transistors [is]are changed between the active and standby states so that active regions of the first and second transistors are [fully]completely depleted simultaneously in the standby state.

5. (*Amended*) A semiconductor device according to claim 4, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said first and second MOS transistors, while a well for the other of the first and second MOS transistors is an N-type well formed in the semiconductor substrate under a P-channel MOS transistor which is the second of said first and second MOS transistors.

7. (*Amended*) A semiconductor device comprising:

a first MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate with the intervention of a buried insulating film,

an element isolating region formed in the semiconductor layer,

a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to a well of the semiconductor substrate, the

well being of the first conductivity type same as [is]that of the other region of the semiconductor substrate directly under the well;

wherein a conductor of the contact portion in the contact region is electrically insulated from said semiconductor layer; and

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltages applied via separate contact regions for both of the first and second transistors [is]are changed between the active and standby states so that active regions of the first and second transistors are [fully]completely depleted simultaneously in the standby state.

8. (*Amended*) A semiconductor device according to claim 7, wherein the well is formed in a surface of the semiconductor substrate which lies under the first MOS transistor formed on the semiconductor layer, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

9. (*Amended*) A semiconductor device according to claim 8, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said first and second MOS transistors, while a well for the other of the first and second MOS transistors is an N-type well formed in the semiconductor substrate under a P-channel MOS transistor which is the second of said first and second MOS transistors.

11. (*Amended*) A semiconductor device according to claim 7, wherein different bias voltages are applied in an operating state and a standby state of a semiconductor circuit including the at least the first MOS transistor, thereby to change a threshold voltage of at least the first MOS transistor.

24. (*Amended*) A semiconductor device comprising:

a PMOS transistor and an NMOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,

a p-type well formed in the substrate for the NMOS transistor and an n-type well formed in the substrate for the PMOS transistor, the p-type and n-type wells being substantially isolated from one another; and

respective contact portions for applying to the semiconductor substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are [fully]completely depleted simultaneously in the standby state, wherein said contact portions are electrically insulated from said semiconductor layer.